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INVESTIGATION OF MINUTEMAN D17B COMPUTER REUTILIZATION

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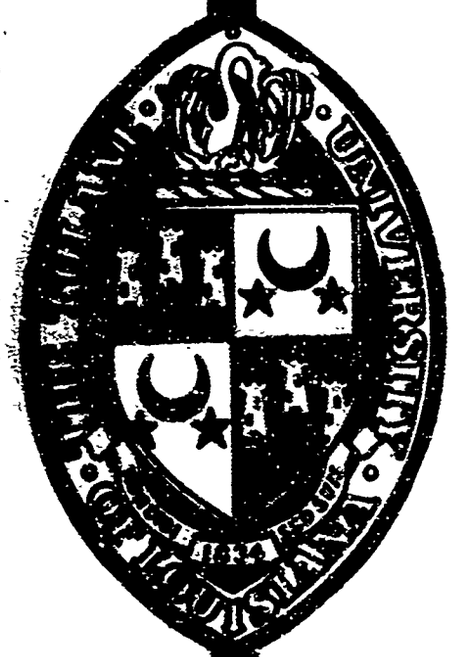
January 1971



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INVESTIGATION OF MINUTEMAN D17B COMPUTER REUTILIZATION

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ABSTRACT

A large number of NS-10Q Inertial Guidance Systems have been declared excess by the USAF which contain D17B digital computers. This report describes the capabilities of these computers and many appropriate applications in which the D17B--a highly reliable and versatile serial-binary minicomputer--can be beneficially employed. Typical areas of application are control, data acquisition, and on-line communications.

A single system design will suffice for the application of several D17B's to similar tasks. While such modifications are very inexpensive, the required interfacing must still be developed. This interfacing is the key to flexible use of these minicomputers; typical I/O devices include: typewriters, teletypes, flexowriters, magnetic and paper tape units, printers, and card readers. Despite the difficulties of limited documentation during the early phases of this investigation and the associated frustration, the D17B is now performing useful functions in the Systems Laboratory at minimal cost.

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1.0 INTRODUCTION

As a result of the current modernization of the Minuteman ICBM force, a quantity of Inertial Guidance Systems, (Model NS-10Q) each costing $234,000 have been declared excess by the USAF. Since over 1,000 of these advanced computer systems from the LGM 30/Minuteman Missiles are scheduled to be declared excess, success of this reutilization project can effect a savings of nearly a quarter of a billion dollars.

NS-10Q systems contain a D17B computer, the associated stable platform, and power supplies. Detailed specifications for the D17B computer are given in Table 1. It is an extremely versatile, multipurpose, serial-binary minicomputer. The Systems Laboratory has acquired several of these systems, and the staff has accomplished installation, troubleshooting, checkout, and hardware modifications necessary to make the D17B portions of these systems completely operational. The high degree of reliability and ruggedness of the computer are evidenced by the strict requirements of the weapons system. Use of the D17B is especially appropriate when high reliability is necessary under extreme environmental conditions such as high shock, acceleration, or vibration that often preclude the use of other computers. The specific application will determine the value of any one characteristic.

Although the NS-10Q system was designed for a real-time guidance and flight control application, the multipurpose computer portion[1,2] can be very useful for many applications once the necessary interface hardware modifications are implemented since the D17B is completely programmable. The instruction repertoire presented in Table 2 contains 39 types of machine language instructions which provide for efficient, flexible programming.

The D17B can be interfaced to existing equipment and it can be shared among several pieces of laboratory or test equipment. A single system design

MANUFACTURER: Autonetics, a Division of North American Rockwell, Inc.
MODEL: D17B
YEAR: 1962
TYPE: Serial, synchronous
NUMBER SYSTEM: Binary, fixed point, 2's complement
LOGIC LEVELS: 0 or False, 0V; 1 or True, -10V
DATA WORD LENGTH (bits): 11 or 24 (double precision)
INSTRUCTION WORD LENGTH (bits): 24
MAXIMUM I/O (words/s): 25,600
NUMBER OF INSTRUCTIONS: 39 types from a 4-bit op code by using five bits of the operand address field for instructions which do not access memory
EXECUTION TIMES:
Add (us): 78 1/8
Multiply (us): 546 7/8 or 1,015 5/8 (double precision)
Divide: (software)
(Note: Parallel processing such as two simultaneous single precision operations is permitted without additional execution time.)
CLOCK CHANNEL: 345.6 kHz
ADDRESSING:
Direct addressing of entire memory
Two-address (unflagged) and three-address (flagged) instructions
MEMORY:
Word Length (bits): 24 plus 3 timing
Type: Ferrous-oxide-coated NDRO disk
Cycle Time (us): 78 1/8 (minimal)
Capacity (words): 5,454 or 2,727 (double precision)
INPUT/OUTPUT:
Input Lines: 48 digital
Output Lines: 28 digital
- 12 analog
3 pulse
Program: 800 5-bit char/s
PHYSICAL CHARACTERISTICS:
Dimensions: 20"high, 29" diam.
Power: 28V dc at 25A
Circuits: DRL and DTL
Double copper clad, gold plated, glass fiber laminate, flexible polyurethane coated circuit boards
SOFTWARE:
Minimal delay coding using machine language
Modular special-purpose subroutines
RELIABILITY: 5.5 years MTBF

Table 1. Minuteman D17B computer specifications.

Numeric Code	Code	Description
00 20, s	SAL	Split accumulator left shift
00 22, s	ALS	Accumulator left shift
00 24, 2	SLL	Split left word left shift
00 26, s	SLR	Split left word right shift
00 30, s	SAR	Split accumulator right shift
00 32, s	ARS	Accumulator right shift
00 34, s	SRL	Split right word left shift
00 36, s	SRR	Split right word right shift
00 60, s	COA	Character output A
04 c, s	SCL	Split Compare and Limit
10 c, s	TMI	Transfer on minus
20 c, s	SMP	Split multiply
24 c, s	MPY	Multiply
30 c, s	SMM	Split multiply modified
34 c, s	MPM	Multiply modified
40 02, s	BOC	Binary output C
40 10, s	BOA	Binary output A
40 12, s	BOB	Binary output B
40 20, s	RSD	Reset detector
40 22, s	HPR	Halt and Proceed
40 26, s	DOA	Discrete output A
40 30, s	VOA	Voltage output A
40 32, s	VOB	Voltage output B
40 34, s	VOC	Voltage output C
40 40, s	ANA	And to accumulator
40 44, s	MIM	Minus magnitude
40 46, s	COM	Complement
40 50, s	DIB	Discrete input B
40 52, s	DIA	Discrete input A
40 60, s	HFC	Halt fine countdown
40 7-, s	LPR	Load phase register
44 c, s	CLA	Clear and Add
50 c, s	TRA	Transfer
54 c, s	STO	Store accumulator
60 c, s	SAD	Split add
64 c, s	ADD	Add
70 c, s	SSU	Split subtract
74 c, s	SUB	Subtract

Table 2. D17B instruction repertoire.

will suffice for the application of a large number of D17B's to similar tasks. It is anticipated that automated systems using the D17B will materially reduce the necessity of constant manual manipulations in several applications areas and the time required to accomplish the demands of an increasing work-load. With automated equipment many more tests can often be performed each day; and highly-skilled personnel are not required. The key to the successful use of the D17B is the interfacing of various peripheral input/output (I/O) devices such as a typewriter, teletype, flexowriter, paper tape unit, card reader, printer, and magnetic tape unit. Continued software development is also needed.

There is an increasing demand for computer systems within DoD, but the products of this rapidly developing technology have a high price tag. This project has demonstrated the potential of constructive reinvestment of USAF funds through a unique effort to develop a flexible, reliable minicomputer system. The D17B can be modified at minimal cost for use in a wide diversity of applications. It can obviously be reutilized effectively as a dedicated, on-line, real-time process controller much as in the original airborne inertial guidance system. Modifications can be made to include such important areas as data acquisition and analysis, on-line communications, data concentration, buffer storage, and preprocessing for analysis and computation by a large-scale computer. The purposes of this report are the following:

1. Ascertain the capability and applicability of the D17B computer for general and control computing applications.
2. Investigate the qualifications of the D17B computer for special-purpose applications such as on-line digital data processing computer interfacing, and peripheral buffering.
3. Identify all required interface hardware to implement any recommended control, general, and special purpose application.

2.0 FUNCTIONAL CHARACTERISTICS

The D17B computer is a multipurpose, serial-binary minicomputer.[3,4] It was designed primarily to solve real-time inertial guidance and flight control problems associated with the Minuteman I missile. The D17B has the following general capabilities:

1. Sampling and processing of input data in the form of control signals, digital data, or pulse-type signals.
2. Logical decision-making and performance of arithmetic operations using an instruction repertoire containing 39 types of machine language instructions.
3. Transmission of output data in the form of analog, digital, and pulse-type signals under program control.

The characteristics of the D17B of specific interest in this investigation will be described. The breakdown of these characteristics along functional subdivisions as identified in Figure 1 is not intended to infer that these elements exist as separate physical entities.

2.1 Central Processing Unit

Since the D17B is a serial-binary computer, simultaneous access to all the bits of a memory location is not needed either for instructions or data. Hence, the arithmetic registers need not be constructed entirely of flip-flops. Instead, they are in the form of circulating loops in memory as illustrated in Figure 2. The D17B has four double-rank arithmetic registers which are accumulator (A), lower accumulator (L), instruction register (I), and number register (N). Because registers (A), and (L) are addressable,

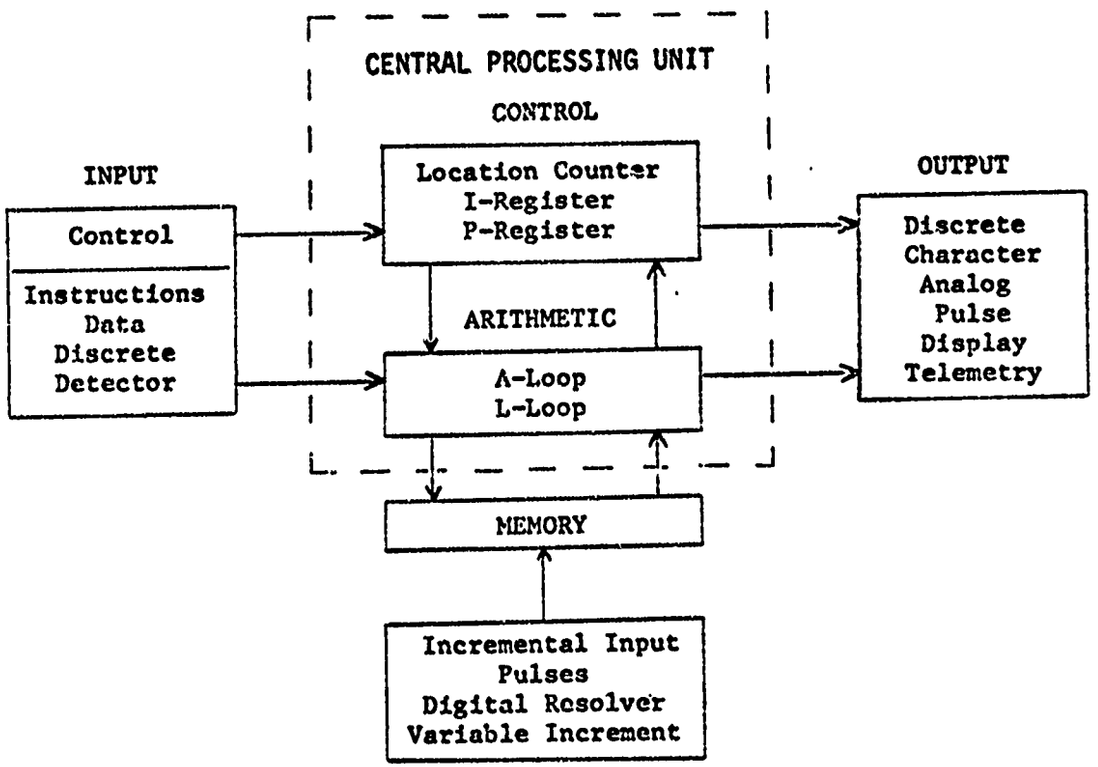


Figure 1. MINUTEMAN D17B computer functional block diagram (conceptual)

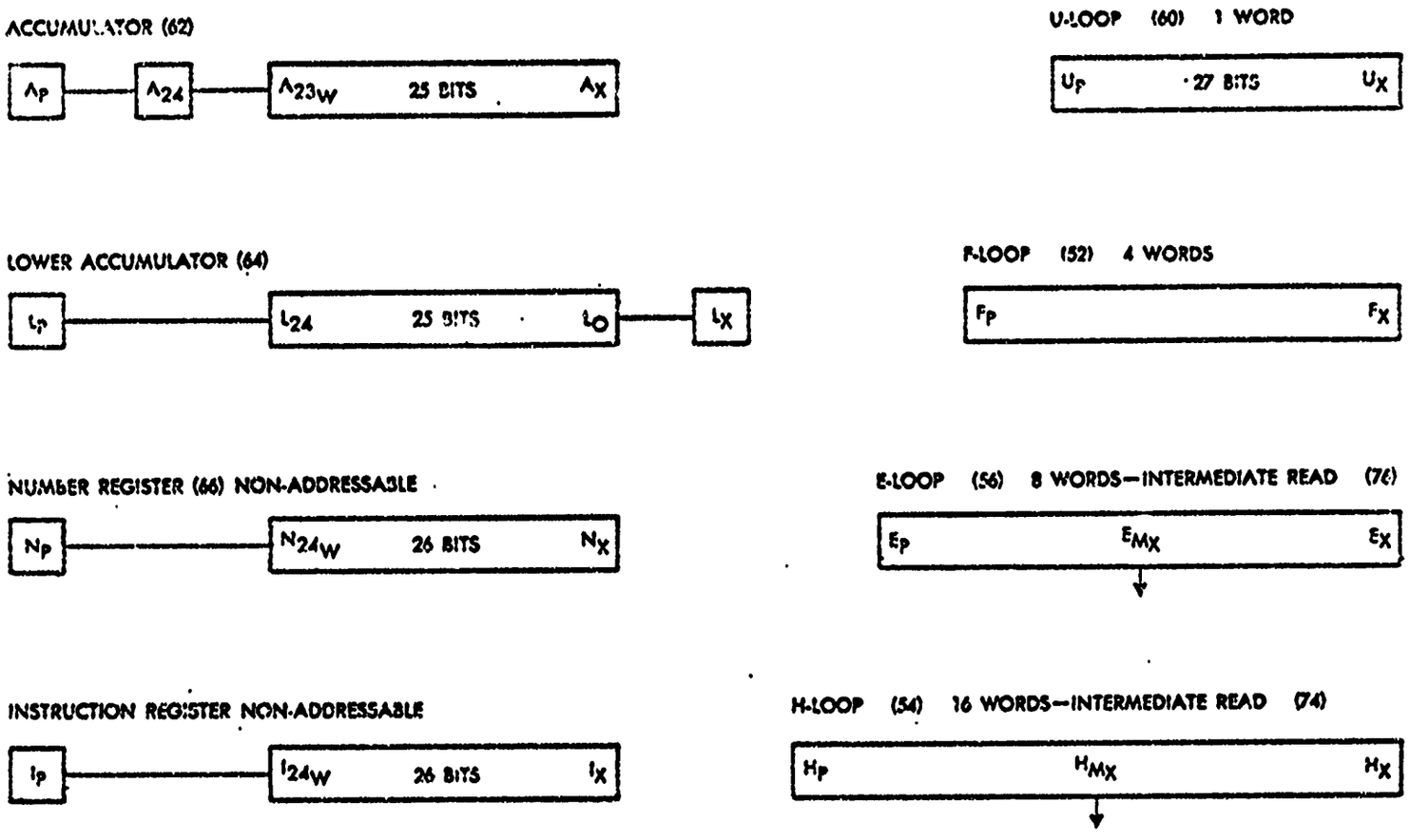


Figure 2. Arithmetic registers and rapid-access memory loops.

they can be used as rapid-access storage in addition to performing normal arithmetic functions. There are two additional non-addressable arithmetic registers which are used without programmer control and one 3-bit pseudo-index (phase) register. The functional locations of these registers and loops are illustrated in Figure 3.

The central processing unit (CPU) has I/O access to four rapid-access memory loops of 1, 4, 8, and 16 words in addition to the main memory which is arranged in 21 channels of 128 words each. Two input buffer loops of 4 words each provide additional input capability from memory.

Programmed data channels cause data transfers into the arithmetic registers. All machine functions are processed and interpreted in the CPU. The memory channel address from which the next instruction is to be taken is determined by the location counter. When the CPU is ready to accept another instruction from memory, the address is specified by the channel address stored in the location counter and the sector address specified in the previous instruction.

The index register can modify the operand channel address of one of the multiply instructions. This register also serves as a selector switch for choosing one of two pairs of inputs to one of the incremental pulse-type input loops and for selecting one of four external positions for each of the three D-A analog voltage outputs.

The accumulator holds the results of all arithmetic operations and serves as an output register for parallel digital data, pulse-type signals, D-A analog voltage outputs, and telemetry data. The lower accumulator is involved in certain arithmetic, input, and logical operations. A real-time clock is provided by internal timing signals derived from the clock channel included in the disk-type memory.

The instruction repertoire listed in Table 2 contains 39 types of machine

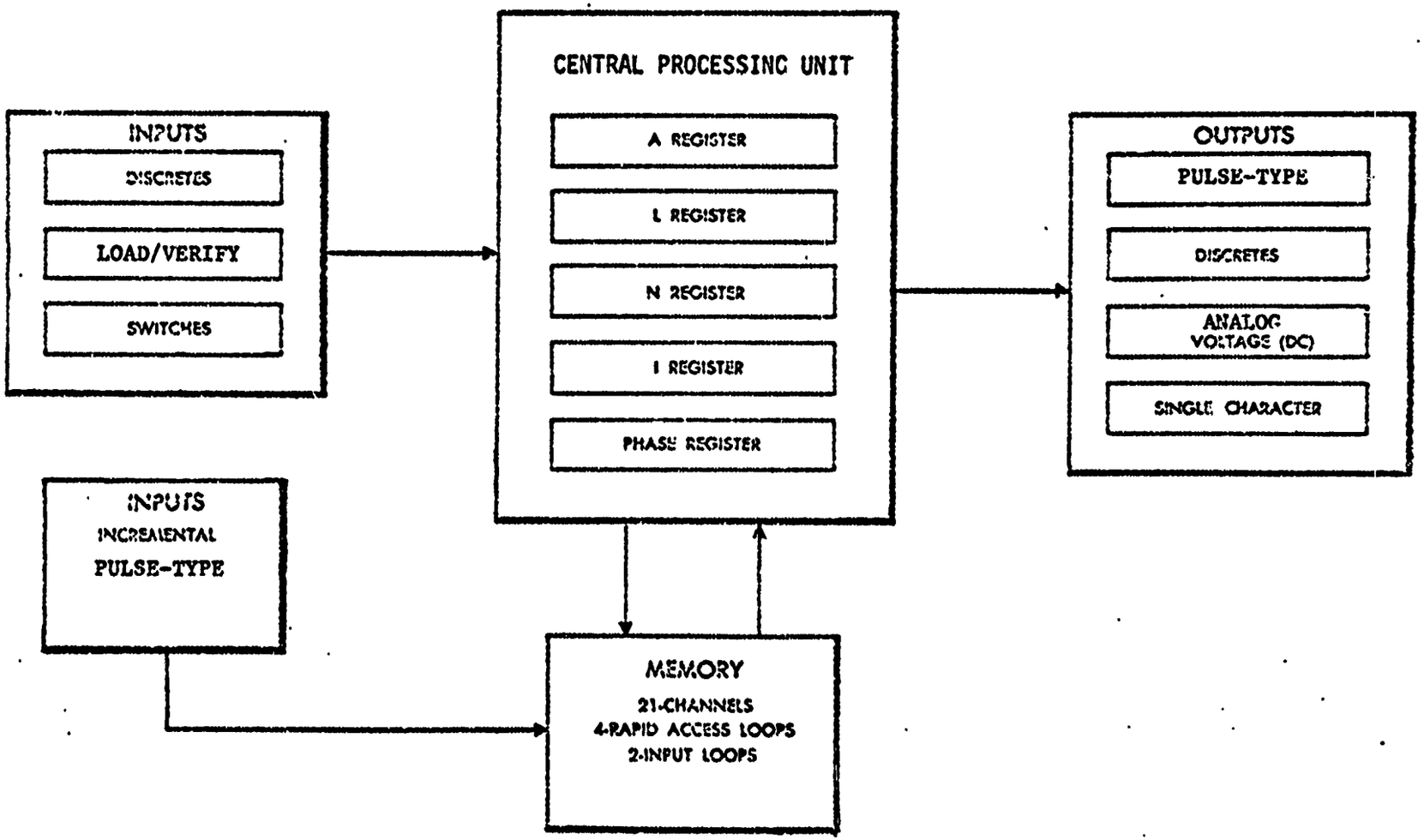


Figure 3. Functional location of arithmetic registers and rapid-access memory loops.

language instructions. Although each type of instruction executed by the D17B differs from one another, the kinds of actions performed occur in a common sequence. This makes it convenient to describe the execution of each instruction as being accomplished in the following five phases which are usually common to delay-type memories:

1. Instruction search (IS)
2. Instruction read (IR)
3. Operand search (OS)
4. Operand read (OR)
5. Execute (EX)

Figure 4 shows that the D17B can perform several of these phases simultaneously with increased efficiency compared to sequential operation. This figure assumes minimal delay coding of instructions which require an execution time of one word time. The advantage of this minimized access timing is that, once a minimal delay coded program is initiated, the effective completion time of any instruction is equal to the basic execution time of the instruction. If random access addressing were used in the D17B, the search operations (IS and OS) could each require up to 128 word times or one disk revoltion of 10 ms. Minimal delay coding places the next instruction at a location which will pass the read head immediately after completion of the current instruction.

The word size for minicomputers ranges from 8 to 24 bits.[5] Providing for direct addressing of the entire memory of the D17B as illustrated in Figure 5 by using a 12-bit operand address field is a feature of considerable value. A typical two-address (unflagged) D17B instruction as illustrated in Figure 6 has three parts: an op code and two addresses. One address identifies the operand which fulfills the same function as the address field in a single address machine, the second is the address mode field S_p which is used to

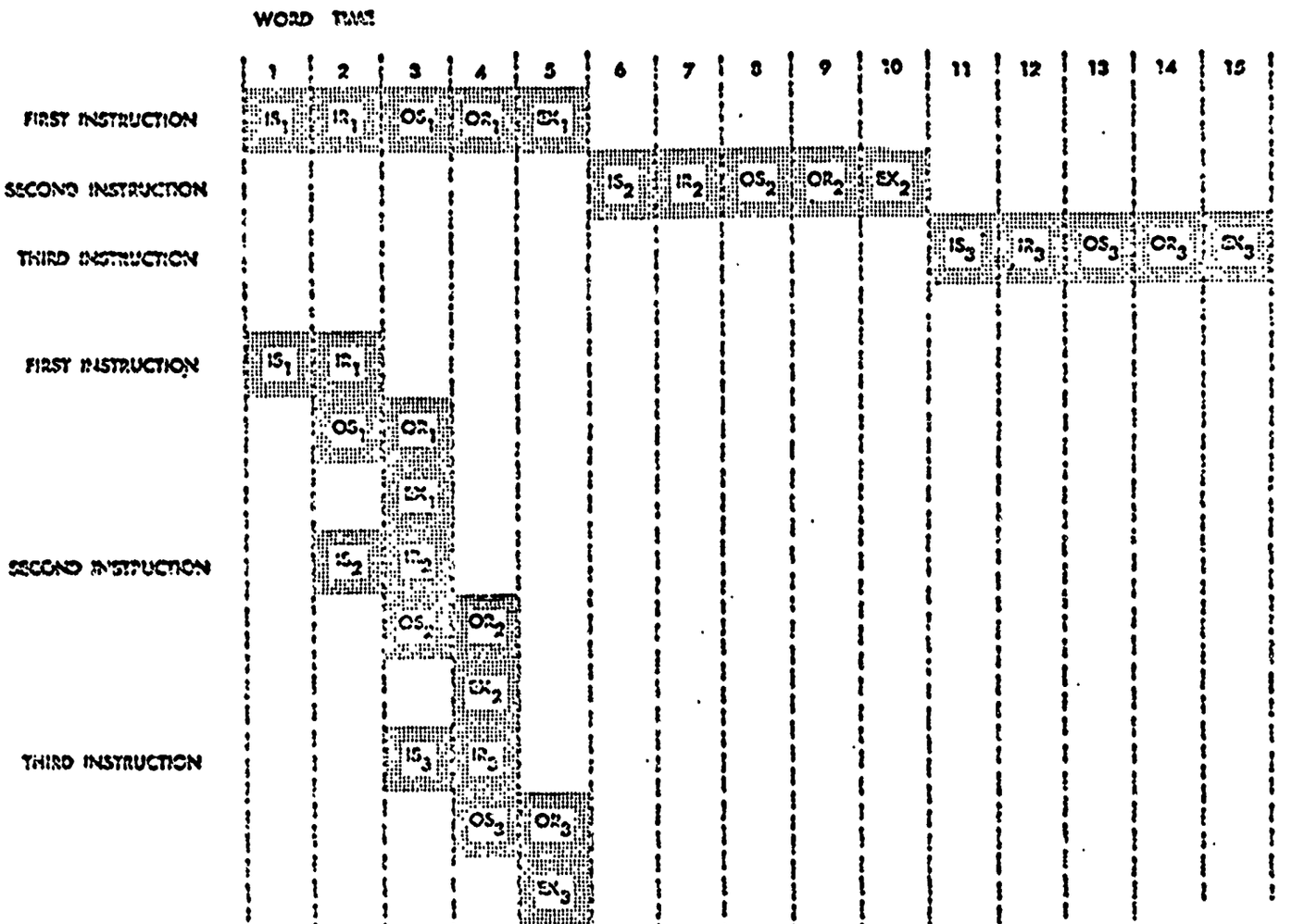


Figure 4. Five phases of D17B instruction execution compared to sequential operation.

UNFLAGGED INSTRUCTION ($T_{20}=0$)

T_P	T_{24} T_{23} T_{22} T_{21}	T_{20}	T_{19} T_{18} T_{17} T_{16} T_{15} T_{14} T_{13}	T_{12} T_{11} T_{10} T_9 T_8	T_7 T_6 T_5 T_4 T_3 T_2 T_1	T_0 T_X
X	OPERATION CODE Op	FLAG F	NEXT INSTRUCTION SECTOR ADDRESS Sp	CHANNEL NUMBER C	SECTOR NUMBER S	X X

FLAGGED INSTRUCTION ($T_{20}=1$)

T_P	T_{24} T_{23} T_{22} T_{21}	T_{20}	T_{19} T_{18} T_{17} T_{16}	T_{15} T_{14} T_{13}	T_{12} T_{11} T_{10} T_9 T_8	T_7 T_6 T_5 T_4 T_3 T_2 T_1	T_0 T_X
X	OPERATION CODE	FLAG	FLAG STORAGE LOCATION S_f	SECTOR OF NEXT INSTRUCTION S_p	CHANNEL NUMBER	SECTOR NUMBER	X X

Figure 5. D17B instruction word format.

UNFLAGGED INSTRUCTION

OP CODE				F	NEXT INSTRUCTION SECTOR							OPERAND													
T_{24}	T_{23}	T_{22}	T_{21}	T_{20}	T_{19}	T_{18}	T_{17}	T_{16}	T_{15}	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	T_7	T_6	T_5	T_4	T_3	T_2	T_1		
OP				F	SP							C					S								
1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	BINARY	
7			4	0	1	7			7			7			6		1	7			7			QUASI-OCTAL	
7			5		7				7			7			7		7				7			OCTAL (MAXIMUM VALUE)	

CODE	RANGE	NUMBERING SYSTEM
SECTOR	000 ϕ 177	SEQUENTIAL OCTAL (0, 1, 2, 3, 4, 5, 6,...177)
CHANNEL	00 ϕ 76	EVEN OCTAL (0, 2, 4, 6, 10, 12,...76)
INSTRUCTION SECTOR	000 ϕ 177	SEQUENTIAL OCTAL (0, 1, 2, 3, 4, 5, 6,...177)
UNFLAGGED INSTRUCTION	0	UNFLAGGED INSTRUCTION
OPERATION	00 ϕ 74	LAST OCTAL DIGIT ENDS IN 0 OR 4

Figure 6. Two-address (unflagged) D17B instruction coding.

specify the address of the next instruction within the active memory channel. One bit (F-flag) in the address mode field permits the use of two alternate address modes. If the flag bit in 0, then an instruction is interpreted as a three-address word. A typical three-address (flagged) instruction as illustrated in Figure 7 has four parts: an op code and three addresses. One address again identifies the operand; the second is used to specify the channel S_F in which the present contents of the accumulator are to be stored; the third is used to specify the address S_P of the next instruction within the next sixteen successive memory locations in the active channel. A program in a single address machine is likely to require much more memory than is required by the D17B.

In the two-address format, the 12 bit operand address is required for direct addressing of the total memory, 7 bits are required to specify the address of the next instruction if any sector within the active channel is allowed, one bit is required for the flag, and the 4 remaining bits are allocated for the op code field. This limits the D17B to 16 unique 4-bit op codes. The 13 instructions that address the memory use these 4-bit op codes and a 12-bit operand address field. Two of the remaining 4-bit op codes are used for instructions that do not reference memory (control, logic, I/O and shifts). A 5-bit portion of the operand address field is used as an extension of the op code.

Considerable expansion of the instruction repertoire appears to be possible. Op code 14 is not used, hence the addition of one instruction that requires access to memory could be considered. Also, there are numerous unused 5-bit op code extensions which could be considered.

2.2 Memory

The delay-type memory is a 6,000 r/min, ferrous-oxide-coated disk as

FLAGGED INSTRUCTION

O_P CODE				F	NEXT INST SECTOR							OPERAND												
T_{24}	T_{23}	T_{22}	T_{21}	T_{20}	T_{19}	T_{18}	T_{17}	T_{16}	T_{15}	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	T_7	T_6	T_5	T_4	T_3	T_2	T_1	
O_P				F	S_F			S_P				C					S							
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	BINARY CODING
7			4	2	1	6		1	7			7			6		1	7			7			QUASI-OCTAL CODING
7				7				7				7					7				7			OCTAL CODING

FLAGGED CHANNEL CODING

T_{19}	T_{18}	T_{17}	T_{11}	CODE	FUNCTION
0	0	0		0 0	IDLE
0	0	1		0 2	(F) 4-WORD LOOP
0	1	0		0 4	(I) TELEMETRY
0	1	1		0 6	(50) HOT CHANNEL
1	0	0		1 0	(E) 8-WORD LOOP
1	0	1		1 2	"L" 1-WORD REGISTER
1	1	0		1 4	(H) 16-WORD LOOP
1	1	1		1 6	(U) 1-WORD LOOP

Figure 7. Three-address (flagged) D17B instruction coding.

illustrated in Figure 8. The disk is driven by a 400 Hz, 3 ϕ hysteresis-synchronous motor. Non-return-to-zero recording is used. The addressable serial memory capacity is 5,454 11-bit (single precision) or 2,727 24-bit (double precision) words. The format of these words is shown in Figure 9. Main memory is arranged in 21 channels of 128 double precision words each. These channels are numbered in even octal from 00 to 50.

Main memory channels are non-volatile in the event of a power failure or if the system is shut down. The clock channel contains a permanently recorded 345.6 kHz sinusoidal signal. Sector information is also permanently recorded on another channel. The total non-destructive readout memory is designed to be completely programmable in conjunction with ground support equipment.

The addressable memory also includes rapid-access loops of 1, 4, 8, and 16 words, two arithmetic registers, and two 4-word input buffer loops for direct data entry. There are two additional non-addressable arithmetic registers. These rapid-access loops and registers are actually reserved memory locations as illustrated in Figure 10.

The memory cycle time is 78 1/8 μs if the memory location is coincident with a read head. This is the time required to read one 24-bit serial word and is defined as one word time. The cycle time for the 1-word registers is one word time. The worst-case cycle times for the 4, 8, and 16-word loops are 4, 4, and 8 word times respectively. The worst-case cycle time for the main memory channels is 128 word times.

Program security or memory protect can be maintained by disabling the write heads to a portion of the memory to effect read-only memory. By enabling these write heads it is possible to perform instruction and address modification under program control.

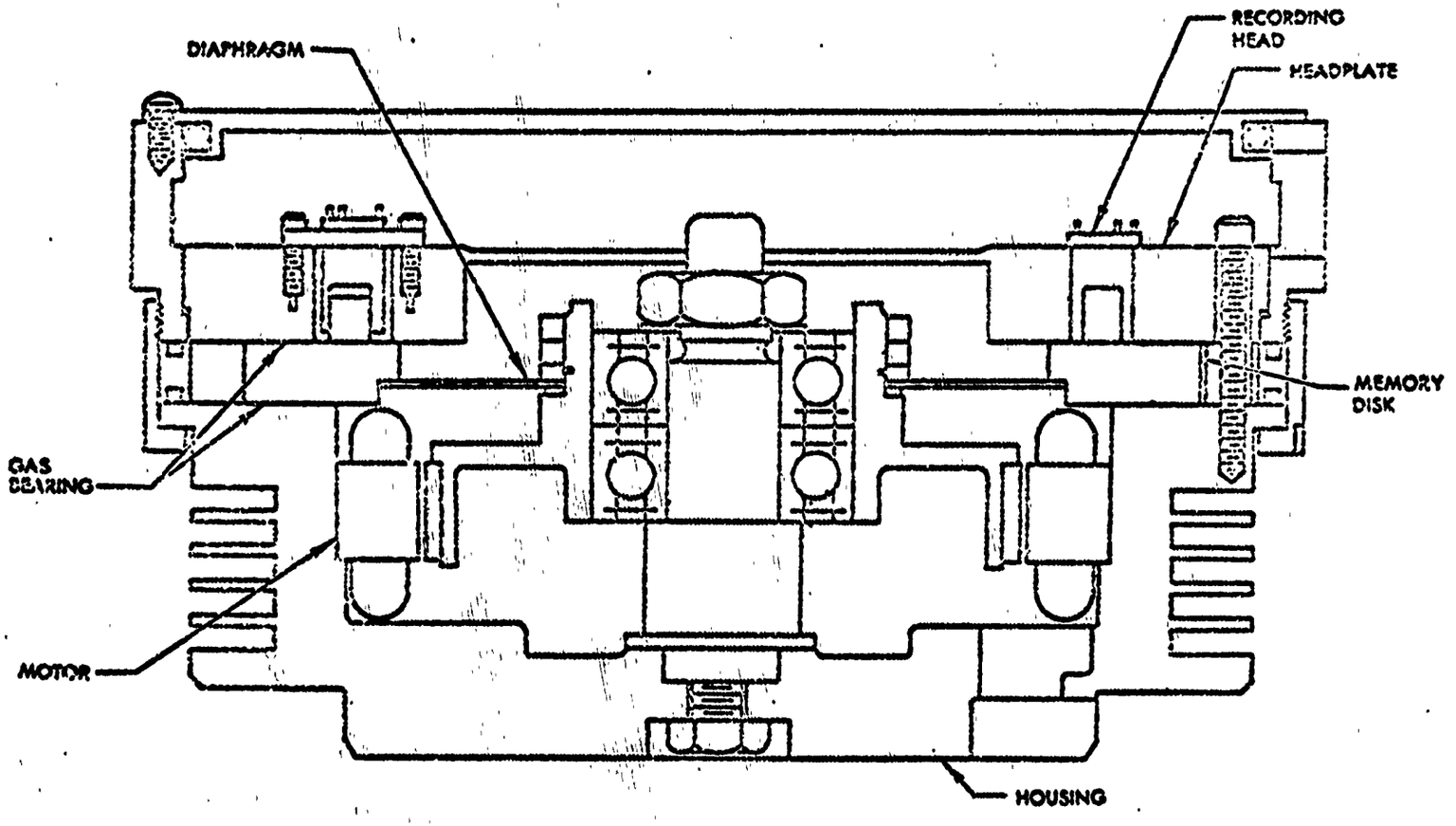
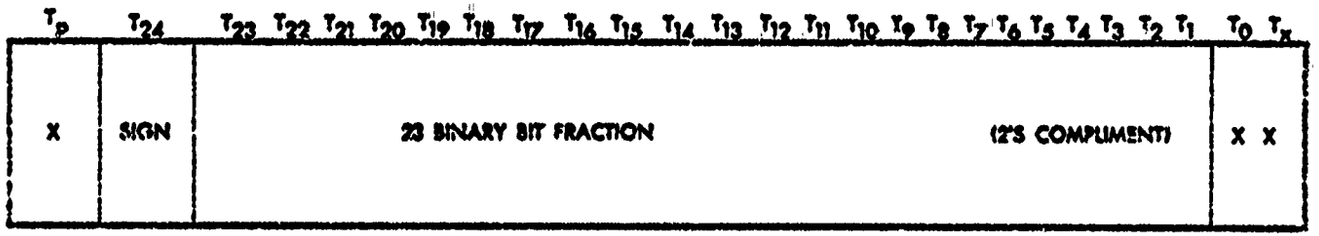


Figure 8. Sectional view of the disk-type memory unit.

WHOLE NUMBER



SPLIT NUMBER

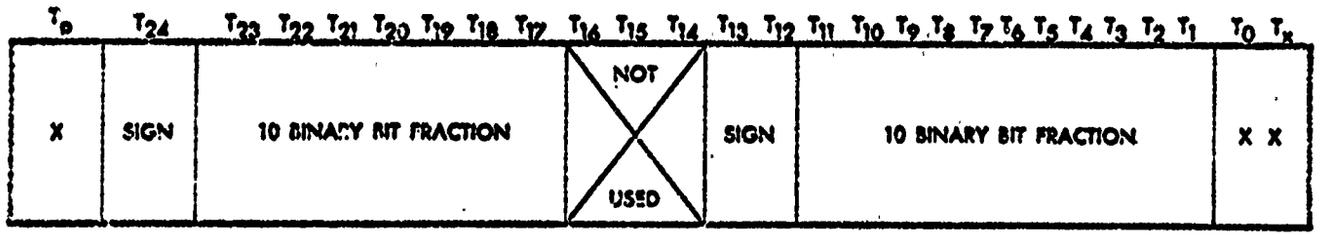


Figure 9. D17B data word format.

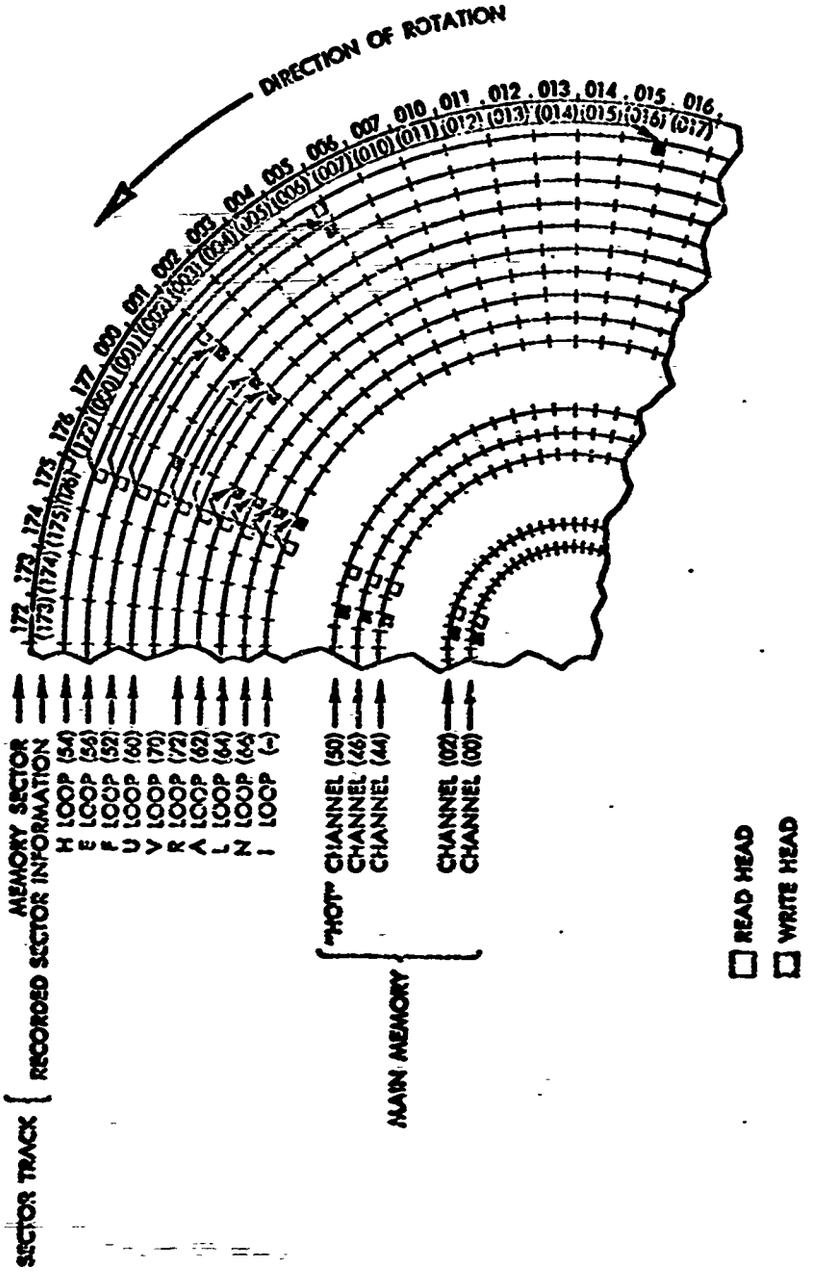


Figure 10. Conceptual diagram of the arrangement of memory loops and registers.

2.3 Input/Output

The program, composed of instruction and data words, is initially punched on cards of paper tape as illustrated in Figure 11, or it is recorded on magnetic tape. This program is then entered into memory. Specific console initializing and interactive inputs must be supplied under operator manual control using push buttons and switches to cause logical synchronization, conditioning of logic circuitry, and sequential state transitions between sub-modes of computer operation. The console control inputs initially cause the D17B to enter the load/verify mode to prepare for entering the program. These console control inputs are listed in Table 3.

Instruction and data characters can be read in during the load/verify mode; sequential memory locations are assumed unless a location control character is present. The maximum rate of loading into or comparing with the contents of memory is 100 words/sec or equivalently 800 characters/sec since each 24-bit word is composed of eight octal characters as illustrated in Figure 12. Negative data must be represented in two's complement form. Control characters read in during the load/verify mode condition logic circuitry to effect appropriate computer operation.

Additional data represented by 48 discrete lines can be entered under program control. One of these discrete lines monitors the detector flip-flop, DR, which can be set by an external source thereby producing a logic signal that indicates the status of external equipment. This function serves as a hardware interrupt. If DR is set, certain discrete outputs are inhibited. DR can be reset under program control.

Incremental inputs of +1, -1, and 0 can be added to the respective contents of eight memory locations in input loops through direct data entry. These inputs are independent of program control. This capability provides for direct

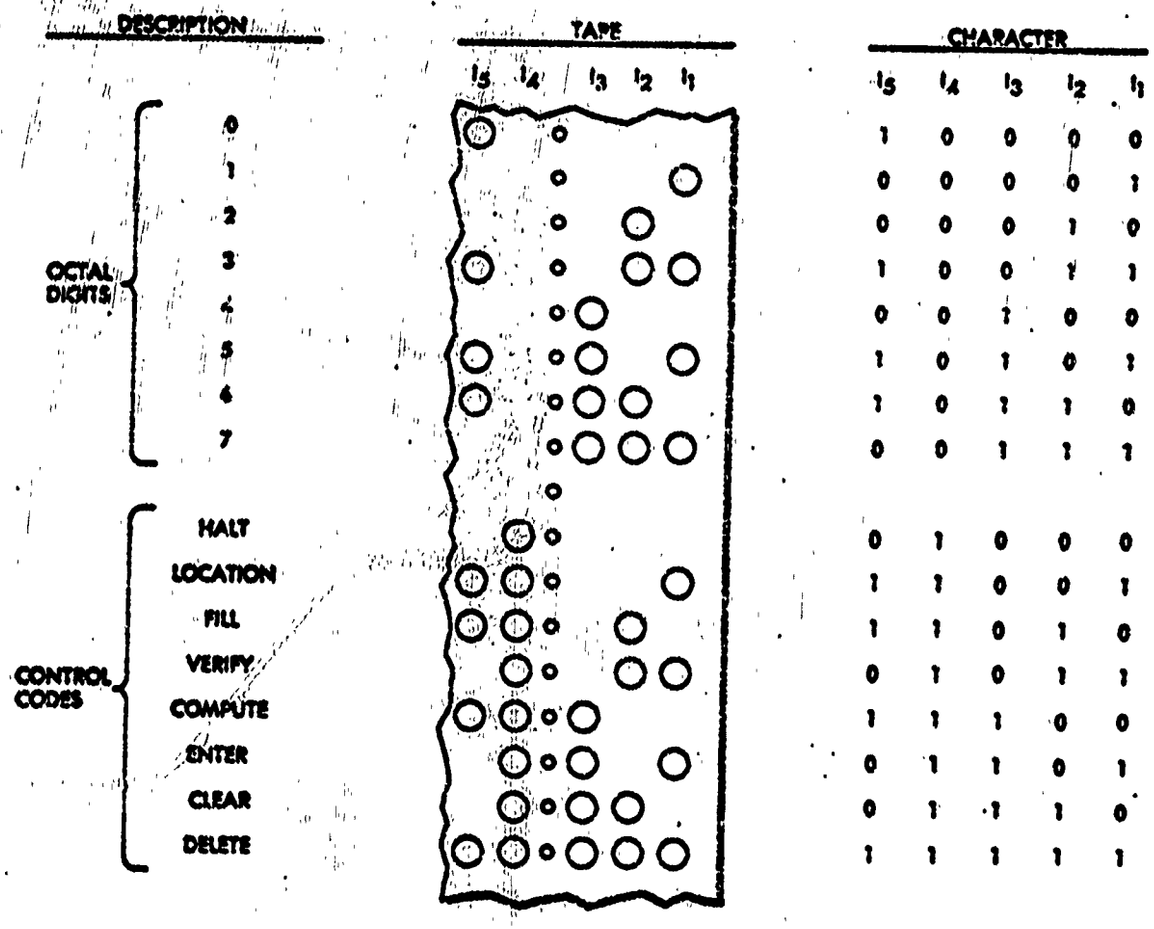


Figure 11. D17B control and octal character codes.

FUNCTION	SYMBOL	POSITION	VOLTAGE	LOCATION
CHARACTER	I1-I5	0	0 V	J7-1 to J7-5
		1	-19 V	(J1-1 to J1-5)
DISCRETE	DDC	ENABLE	-25 V	J7-14
		DISABLE	0 V	(J1-23)
FILL	FSC	NORMAL	0 V	J8-24
		FILL	-19 V	
HALT'	KHC'	RUN	-19 V	J7-17
		HALT	25 V	(J1-91)
RESET	MRC	NORMAL	15 V	J7-15
		RESET	-19 V	(J1-90)
RUN'	KRK'	HALT	-19 V	J8-16
		RUN	25 V	
SINGLE'	KSK'	NORMAL	-19 V	J8-15
		Single	25 V	
TIMING	TC	0	0 V	J8-38
		1	-25 V	
TIMING'	TC'	0	-25 V	J7-6
		1	0 V	(J1-6)
WRITE	EHC	ENABLE	25 V	J7-16
		DISABLE	-19 V	(J1-93)

Table 3. D17B console control signals.

SIGN	WHOLE NUMBER																						
T_{24}	T_{23}	T_{22}	T_{21}	T_{20}	T_{19}	T_{18}	T_{17}	T_{16}	T_{15}	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	T_7	T_6	T_5	T_4	T_3	T_2	T_1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7			7			7			7			7			7			7			7		

SIGN	10 BIT BINARY FRACTION										X	X	SIGN	10 BIT BINARY FRACTION									
T_{24}	T_{23}	T_{22}	T_{21}	T_{20}	T_{19}	T_{18}	T_{17}	T_{16}	T_{15}	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	T_7	T_6	T_5	T_4	T_3	T_2	T_1
1	1	1	1	1	1	1	1	1	1	1	X	X	1	1	1	1	1	1	1	1	1	1	1
7			7			7			6			3			7			7			7		

Figure 12. D17B data word coding.

digital integration of eight functions, five of 11-bits each, two of 24-bits each, and one of 48-bits. Variable increment-type inputs can also be added to the respective contents of memory locations in input loops through direct data entry. These inputs enter the computer on two sets of three lines. One line indicates the sign, and the other two mutually exclusive input lines indicate increments of one or four. The state of the phase register determines which of the two pairs of inputs is selected. A pulse-type input can be added to the contents of a specific memory location at the maximum rate of 1000 pulses/sec.

The variety of output transfers available from the D17B under program control include 3-bit, 4-bit, or 8-bit parallel data channels, discrete logic signals, pulse type signals, 24-bit serial words, and analog signals. Parity or verify error outputs are also provided as hardware-controlled features. Specific discrete logic signals are disabled by a hardware interrupt if DR is ON.

With these output features, the D17B can output data to an automatic typewriter, light indicators, audible alarms, and other off-on devices. An array of light indicators can be used to display data in various coded forms. Continuous analog output signals can be monitored on a meter, or a permanent and continuous record can be preserved by using a strip chart recorder. Other peripheral devices can be used to prepare punched cards, punched paper tape, or magnetic tape for subsequent data entry into the D17B or another computer for later processing off-line.

3.0 PHYSICAL CHARACTERISTICS

The Inertial Guidance Systems (Model NS-100) of the LGM 30/Minuteman ICBM Missile contains a D17B minicomputer, the associated stable platform, and

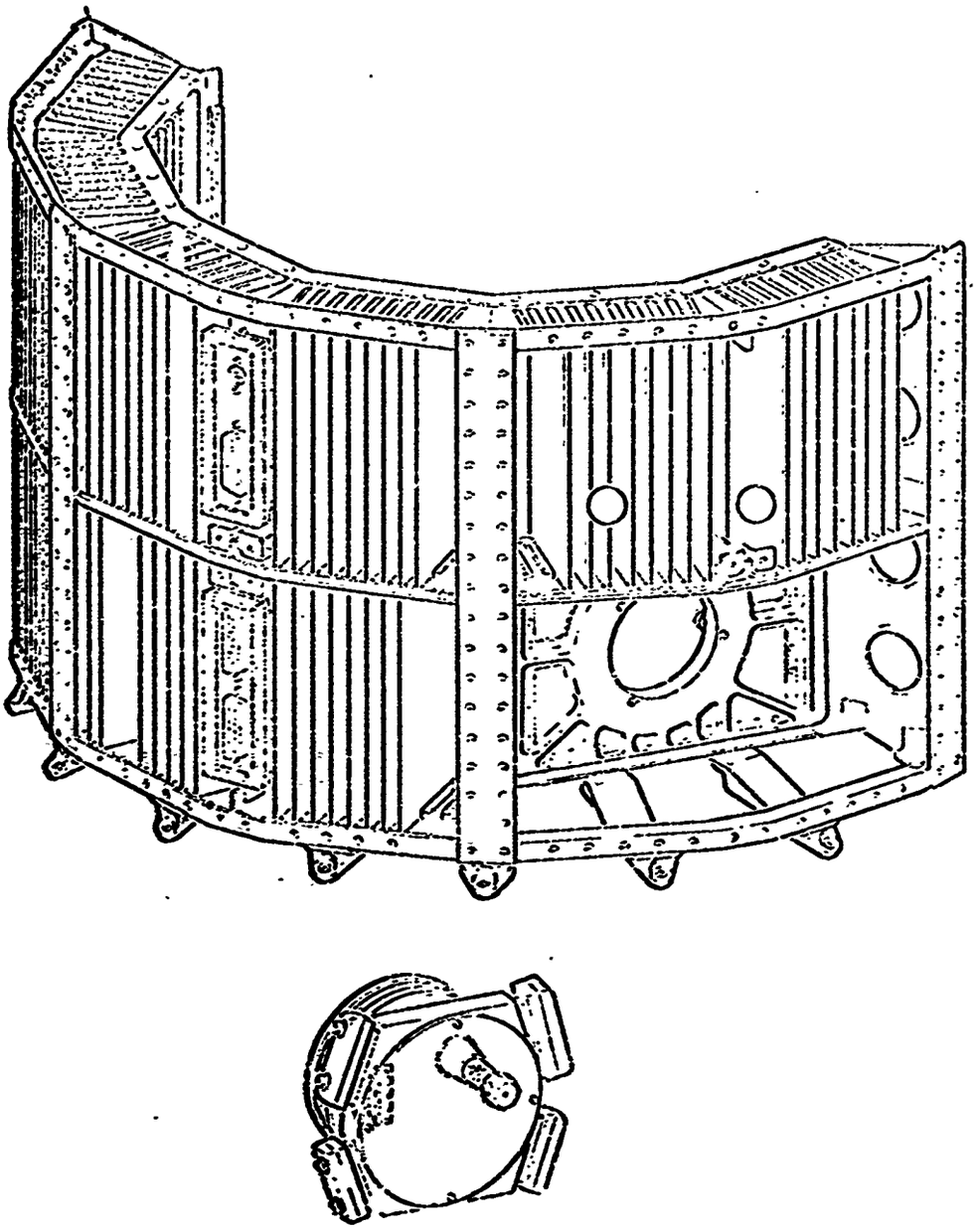
power supplies. The D17B, built by Autonetics, a division of North American Rockwell, occupies 180° of the chassis structure of the NS-10Q as shown in Figure 13. The power supply section occupies the other half of the chassis structure toroid. The outer body skin which provides the NS-10Q the capability of becoming an integral part of the missile frame may be unbolted and removed when the NS-10Q is to be reutilized for other purposes. Removal of this body section will have no effect on the operation of the D17B. The NS-10Q is located just beneath the payload in the nose cone.

A 28V dc regulated power supply capable of supplying 25A must be provided for operation of the computer. Other required voltages are obtained by converting 28V dc into secondary power using solid-state circuitry. The current drawn from the 28V dc supply will vary from 0 to 25A with a steady state value of 19A referred to as full load.

The secondary power requirements include 400Hz, 3ϕ, and various dc voltages as shown in Figure 14.

The D17B is 20 in high, 5 in deep, 29 in diameter, and weighs approximately 62 lbs. Components include approximately 1521 transistors, 6282 diodes, 1116 capacitors, and 509¼ resistors. These components are mounted on double copper clad, engraved, gold plated, glass fiber laminate. There are 74 of these circuit boards. They have been coated with polyurethane.

The design of the D17B placed a premium on reliability since there is no second chance when an airborne computer controlled mission is executed.[6,7] Hence, DRL logic was used extensively rather than DTL except where gain was required. Extensive use was made of silicon and mesa-germanium semiconductor devices in this fully solid-state computer. A logic level of 1 or True is represented by approximately -10V, and a 0 or False by approximately 0V.



MEMORY UNIT

Figure 13. MINUTEMAN D17B MINICOMPUTER SKETCH

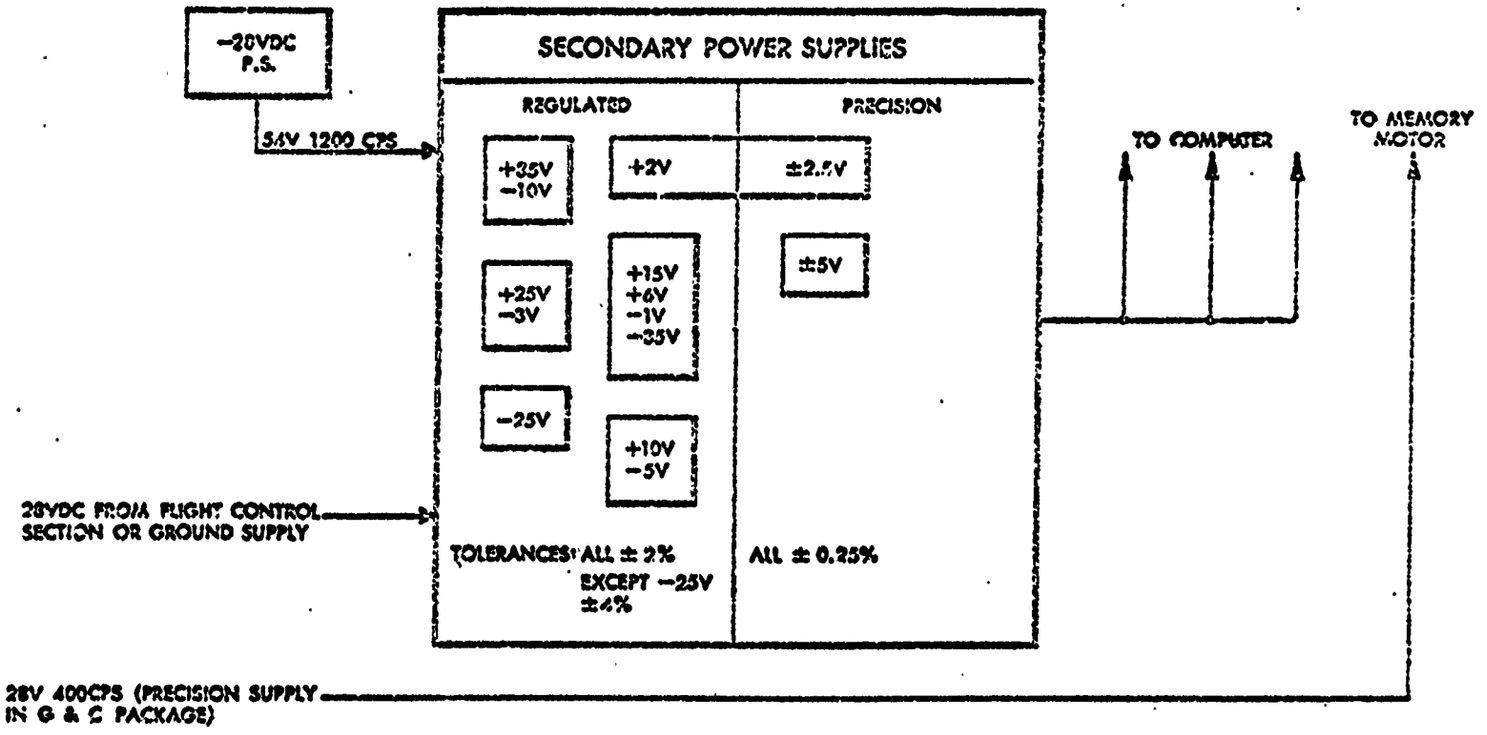


Figure 14. D17B power supplies.

4.0 OPERATIONAL CHARACTERISTICS

The logical power of general-purpose computers is uniquely common to all, but speed of execution, memory size, cost, reliability, and ease of communication (convenience to the user) differ widely. Size and weight limitations, a high degree of reliability and strength, plus program requirements dictated a small, slow, serial memory for the D17B. However, many minicomputers have less than half the memory of the D17B.[7,8] Requirements for real-time operation imply the need for the D17B to sequentially perform its assigned tasks fast enough so that all tasks are accomplished during a given period of time and yet slow enough to ensure accurate noise-free computation.[9]

In addition to the usual capabilities common to general-purpose computers, it can be seen in Figure 15 that the D17B has analog, pulse-type, and serial output systems. Parallel or multiprocessing such as the simultaneous execution of two identical single precision add, subtract, or multiply instructions is another unusual operational capability.

The need for store instructions arises frequently because of the need to preserve intermediate results while some related intervening series of operations is being performed as in the evaluation of a general polynomial. Simultaneous execution of a store operation is possible on the D17B coincident with the initiation of other operations without requiring an additional instruction. The contents of the accumulator will be stored in the channel specified by the S_P address as illustrated in Figure 16.

Instruction and address modification give the program the ability to branch to alternative sequences of instructions under program control as a result of calculations in addition to the use of conditional and unconditional branching instructions. Bit manipulation is also possible if the accumulator is masked by using the logical AND instruction.

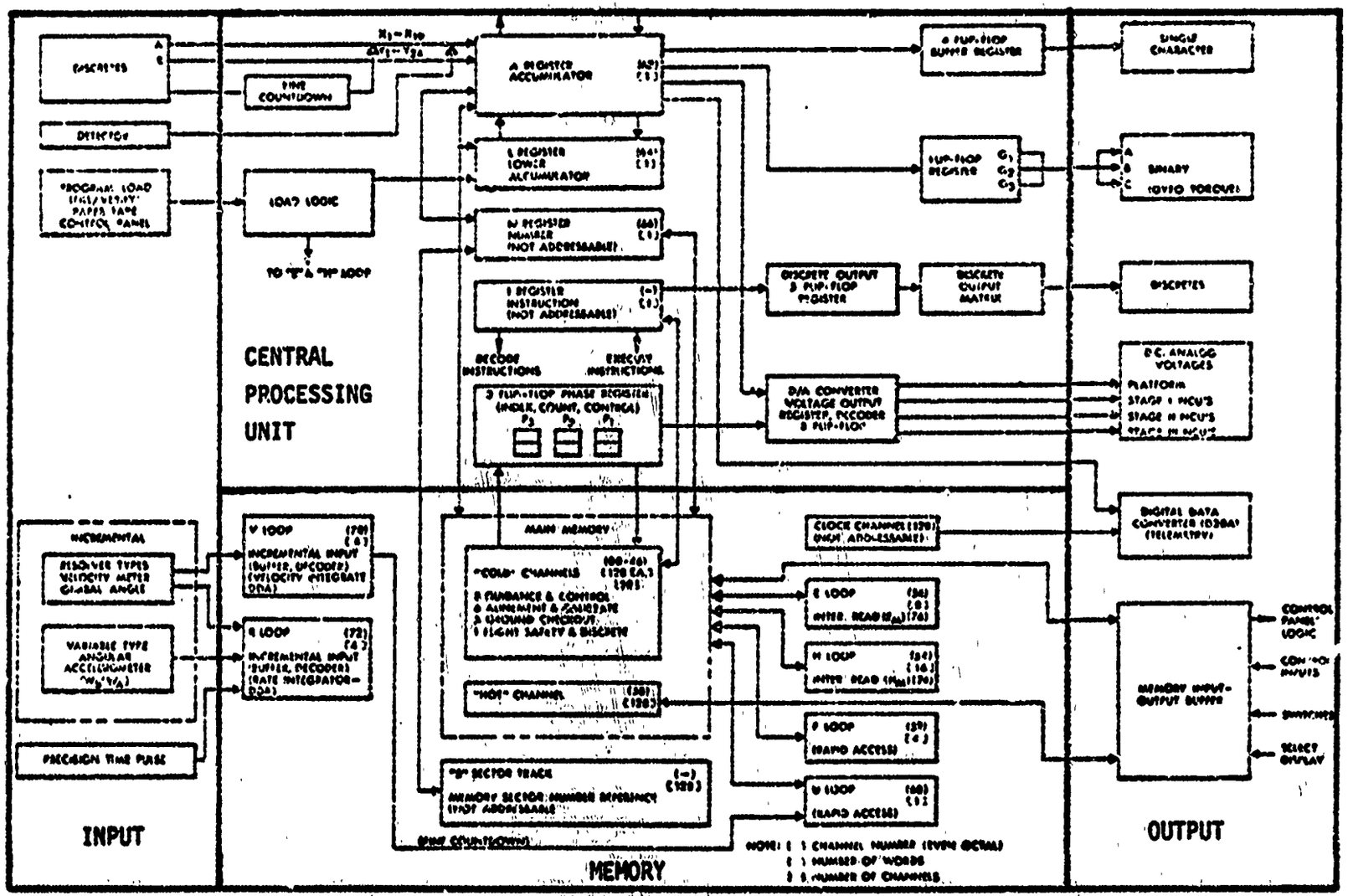
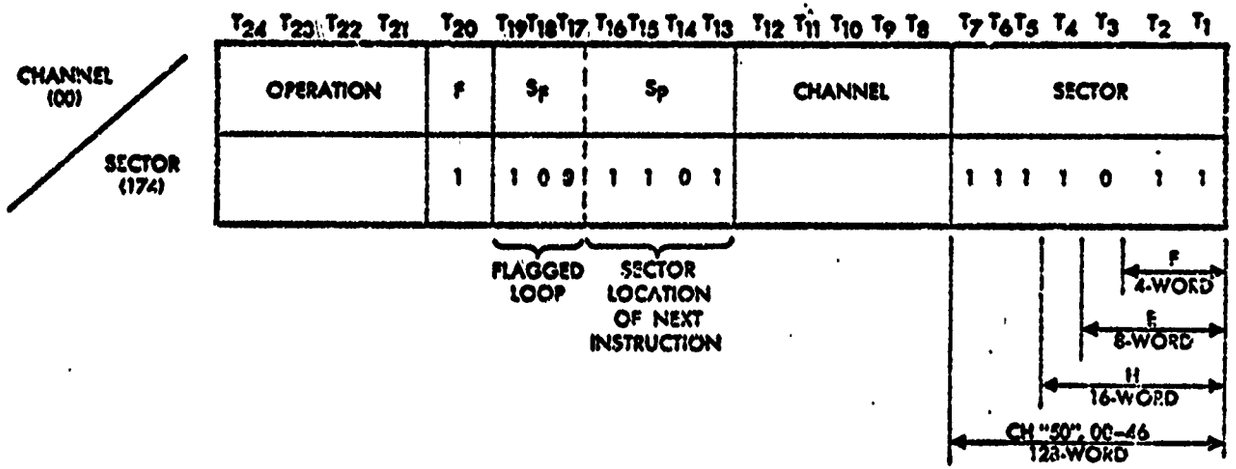


Figure 15. D17B functional data flow diagram.



① THE NEXT INSTRUCTION WILL COME FROM ONE OF THE NEXT 16 SECTORS AFTER OPERAND AGREEMENT.

② THE CONTENTS OF THE A-REGISTER WILL BE COPIED INTO THE FLAGGED CHANNEL UPON EXECUTION OF THE FLAGGED INSTRUCTION. THE WORD LOCATION OF THE FLAGGED CHANNEL, WHERE THE CONTENTS OF THE A-REGISTER WILL BE STORED IS DEPENDENT UPON THE APPROPRIATE OPERAND SECTOR BITS.

Figure 16. Flag store instruction sector coding.

Compiler routines which have the advantage of reducing programming effort are not currently available for the D17B. The relative inefficiency of memory requirement for compiler produced programs compared with programs writt /in machine language makes the on-line compiler approach questionable at t' ; time.[10,11] The modular approach to the writing of special-purpose sub tines such as required for I/O operations can result in considerable sav gs in time and effort. Certain features such as dedicated I/O registers uce the programmer's housekeeping task. The use of rapid-access memory loops provides programming versatility and efficiency that help to overcome the limited speed of execution and memory size of the D17B.

5.0 CAPABILITY OF THE D17B COMPUTER FOR GENERAL AND CONTROL COMPUTING

Although the D17B does not provide all the desirable features of large general-purpose machines, it does resemble them functionally and it possesses a number of similar features. It is a versatile multipurpose computer capable of solving a wide range of problems;[12,13] however, it has limited capability both in storage capacity and computation speed. Unlike the emphasis placed on efficient processing of many different programs on a large general-purpose machine, the multipurpose D17B is better suited to dedicated or fixed tasks that can be served effectively by economical use of the available memory and speed of execution.[14,15]

Consequently, the D17B like commercial minicomputers with small memories, is not well suited for general-purpose computing when compared to a large computer.[16] General-purpose computation in minicomputer terminology refers to stand-alone operation. Some minicomputers are used as stand-alone computers for scientific and engineering use, but most are used in real-time applications such as control, data acquisition, communication concentrators and processors,

peripheral controllers and preprocessors for large computer systems, display controllers, buffer memories, bio-medical monitoring, automated testing, automated instrumentation and telemetry.[17-34]

In a practical sense, the capability for general computing is determined by the ability to perform a large variety of calculations. This is determined basically by the instruction set. Available subroutines simplify the programming, and assemblers and compilers simplify the task further. The goal in providing general-purpose software for the D17B is to minimize the amount of time, effort, and knowledge required for a user to arrive at a point of useful return for his investment in the development of the D17B. But, generality always comes at a price. The D17B is limited at present to a small number of real-time, special-purpose machine language programs.

The apparent lack of speed is not such an important factor when the D17B is used as a dedicated control computer since much computing speed available in a large general-purpose computer is commonly lost in system overhead and I/O.[35,36] Furthermore, the 4-bit and 8-bit parallel output data channels available on the D17B should prove to be very advantageous in communications systems that operate on 8-bit ASCII characters, because the overhead operations of packing and unpacking are minimized. The 24-bit double precision data word used on the D17B appears to have considerable utility for computation associated with these 8-bit codes for character representation which are now becoming standard. Therefore, the 24-bit word of the D17B not only offers more precision than most minicomputers, but it provides for outputting 8-bit submultiples.

Computer control applications may include monitoring and data processing, start-up and shut-down procedures, and optimal control. The main attributes of computer control are computational speed, storage capability, and decision-making ability. If sufficient computational speed is available, optimal control

can be accomplished. The storage capability provides for economical and efficient data recording and processing. Decision-making ability provides the capability for direct digital control.

A direct digital control system must provide a means for measuring the condition to be controlled, compare the measured value with a desired value, and automatically cause the two values to agree. Data logging can be performed as one phase of the control operation. Feed-forward control requires the solution of equations which represent a predictive mathematical model. A control computer can also be used for supervisory functions such as start up or shut down operations. Direct digital control requires that each variable be compared in turn with the desired values.

Logical decisions and constraints can be employed in computer control, and the results of intermediate calculations and control actions can be recorded to produce a historical file. The general-purpose capabilities of the D17B permit the control program to be modified and expanded within the limits of memory capacity to fit system growth, new instruments, or changing control policy. The versatility available with a computer control system involving a general-purpose computer is an important consideration.

If the D17B is to be used for control computing applications, it must be capable of not only performing control calculations, but a number of other essential functions also. For example, raw input data are generally subjected to individual limit checks to detect instrument failures or out-of-normal conditions, averaged or smoothed to minimize the effects of random variations, and then recorded or used in calculations. As a typical example of a limit check in terms of D17B instructions, the following could be executed:

1. DIA - data input to A
2. MDM - replace the contents of A by the negative of the present magnitude of the contents of A

3. ADD - add the limit tolerance to the contents of A

4. TMI - transfer on minus

These four instructions would accomplish the limit check by performing a conditional branch. Similar operations could be equally useful for general or special-purpose computing.

It is appropriate that the D17B be considered for dedicated control applications involving control over a single unit or a limited portion of a process. Such an application may not only be appropriate considering the limited memory and execution speed of the D17B, but the system reliability consideration makes D17B's idealy suited to such tasks. Process-wide control may require several interconnected D17B's. The real-time aspect of control applications is compatible with the current requirement of machine language programming for the D17B.

Considerable benefit can be gained by using dedicated computers which decentralize system design and simplify software requirements. The major advantages of using several dedicated control computers are the complete independence of each unit from failures in other units and the reduced sophistication required to program the computations. Dedicated control computers make automated start-up a practical consideration.

Since A-D and D-A converters and multiplexers are required for each computer, the use of several dedicated D17B's could represent too large an expenditure in conversion equipment. But, because conversion and other subsystem costs have been reduced considerably, the use of several dedicated computers appears to be feasible. Delays caused by breakdown can be avoided by using a dedicated on-line machine, and there is no question about program security.

As new instruments are added and as knowledge of a process increases,

better control policies can be developed. Hence, control programs are constantly in need of change. Also, the characteristics of the process will often change as its operation is improved through computer control. Because of these factors, the programmable feature of the D17B is extremely desirable as well as its flexible I/O capabilities, which can accomodate a variety of control devices. The D17B can provide digital, pulse-type, and analog output signals under program control for manipulating process variables. This flexible I/O capability provides for efficient interaction between the D17B and the devices being controlled.

6.0 CAPABILITY OF THE D17B FOR SPECIAL-PURPOSE COMPUTING

Certain special-purpose applications such as on-line digital data processing, computer interfacing, peripheral buffering, and data monitoring require very little CPU sophistication, limited arithmetic capability, and perhaps low-speed performance compatible with the D17B specifications. The dominant requirement of many special-purpose computer applications relates to the I/O architecture as is the case for control applications. Section 2.3 describes the I/O capability of the D17B. The importance of I/O channels is particularly significant where data is being transmitted continuously between the computer and peripheral devices.

On-line digital data processing often requires that analog information be converted to digital form using an A-D converter. With the 24-bit double precision word of the D17B, the output from two 12-bit A-D converters can be inputted simultaneously under program control. The required speed of I/O transfers and airthmetic for special-purpose data acquisition can be much slower than for control applications because real-time analysis and control response commands are not necessary. Hence, the D17B with functional capabilities as described in Section 2.0 is flexible enough to be used in these special-purpose areas formerly requiring special-purpose computers. As requirements change, the D17B can easily be re-programmed. In such fields as medical research, biological studies, and experimental physics, the D17B can be programmed to control the monitoring, measuring, and recording of a veriety of quantities such as pressures, flow rates, EKG, and heart rate. Automation of chemical laboratory instruments such as chromatographs, spectrometers, and AutoAnalyzers using the D17B also appears feasible. Calculation of desired parameters, recording of results, and graphic display are appropriate applications areas for this computer. Simultaneous measurements of several

quantities are possible through the use of sample-and-hold devices, a multiplexer, and an A-D converter.

A flexible, reliable, mobile data monitoring system can be developed using the DL7B computer with interface to any of the following: operational amplifiers, sample-and-hold devices, multiplexers, analog-to-digital converters, digital voltmeters, counters, CRT displays, plotters, programmable signal generators and power supplies, transducers, and sensors. This combination will provide for the automatic testing of electronics components, IC, logic cards, complete logic assemblies, and other devices and circuits. Programmed transducer testing and high-quality data collection of signal characteristics such as amplitude, current, and phase which can be accomplished at high speeds have significant advantages over manual methods. These techniques are also applicable to non-destructive testing as employed in the inventory of aircraft parts based on the characteristics of the steel as represented by the electrical output of spectrometer-type instruments.

On-line communication is also an important applications area to be considered for the DL7B. A data concentration buffer storage system for teletype and other low speed I/O devices can be developed. Programmed multiplexing of parallel information for serial transmission over a narrow-band communication channel is possible since the DL7B can provide for changing the scan rate. Preprocessing for analysis and computation by a large-scale computer will also be an appropriate consideration.

7.0 D17B RELIABILITY

One aspect of the applicability of the D17B for general, control, and special-purpose applications relates to the reliability of the computer. Mr. Ray E. Close, System Manager, IGM 30 Systems Management Division, Hill AFB, stated at the first Minuteman Computer Users Group meeting in Anaheim, California on June 12, 1970, that the average MTBF for the over 1,000 D17B's had exceeded 5.5 years.

During the time that the D17B has been operating in the Systems Laboratory at Tulane University, a few failures have occurred. These failures were created by occasional inadvertant, improper procedures when measurements were being taken under difficult circumstances. For normal laboratory operating conditions, the D17B can be powered up and shut down frequently without experiencing malfunctions as has been the case during the past 15 months of operation in the Systems Laboratory.

Thus, the reliability of the D17B will hopefully reduce the occurrence of equipment breakdowns and the need for technical maintenance personnel and the associated maintenance costs once the system is in operation. This is partly because of the use of high reliability components. Also, since the D17B is available to authorized government agencies and contractors for use on contracts or grants on a non-reimbursable basis, there will be insignificant cost increase with usage. And, with the assistance of the MCUG, it is expected that many users will take over complete system responsibility including maintenance. It is expected that less-skilled technicians can be trained to provide the necessary service. The very high MTBF of the D17B should be considered when planning a minicomputer control system for a process which should not be interrupted.

8.0 HARDWARE INTERFACE DEVELOPMENT

The hardware that has been developed during this investigation consists of the I/O interface required to connect the D17B to an electric typewriter and a paper tape reader/punch. The peripheral device is a Friden Flexowriter, Model SPD. This device is commonly avaiable as government excess ADP equipment. Figure 17 is a schematic of the interconnections between the Flexowriter and the D17B. Interface design requires electronic and functional considerations.

Figure 18 is a block diagram of the electronic circuits required for conditioning the input signals to the D17B from the Flexowriter. These circuits are required for the purposes of suppressing noise, changing voltage levels, inverting the signals from positive to negative logic, shortening the pulses, delaying the timing pulse, and generating the complement. Figure 19 is a block diagram of the electronic circuits required for conditioning the input signals to the Flexowriter from the D17B. These circuits are required for stretching or storing the information pulses, delaying the timing pulse, changing voltage levels, and inverting the signals from negative to positive logic.

The following should be considered in planning for a D17B system.

1. Shipping for D17B and I/O devices, available through DSA.
2. Interfaces for connecting peripheral I/O devices to the D17B.*
3. 28V dc power supply rated at 25A.
4. Air duct and circulating blower (air at 75° for less).
5. Operator control panel.*
6. Engineering effort and labor to install and check out the D17B.*
7. Software development, trouble-shooting, and maintenance.*

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*Available through the Minuteman Computer Users Group.

A. FLEXOWRITER CODE MODIFICATION:

KEY	FUNCTION	FLEXOWRITER OUTPUTS I1	I2	I3	I4	I5	MODIFIED FLEXOWRITER OUTPUTS I1	I2	I3	I4	I5
SPACE	0	0	0	0	0	1	0	0	0	0	1
↑	LOCATION	1	1	0	1	1	1	0	0	1	1
=	ENTER	1	1	0	1	1	1	0	1	1	0
,	FILL	0	0	0	0	1	0	1	0	1	1
↑	COMPUTE	0	0	0	0	1	0	0	1	1	1
.	VERIFY	1	1	0	1	1	1	1	0	1	0
?	CLEAR	1	1	1	0	0	0	1	1	1	0
	HALT	1	0	0	0	0	0	0	0	1	0

B. INTERFACE:

CHANGE VOLTAGE LEVELS FROM 0V/90V TO 0V/-25V
AND/OR FROM 0V/-10V TO 0V/90V.

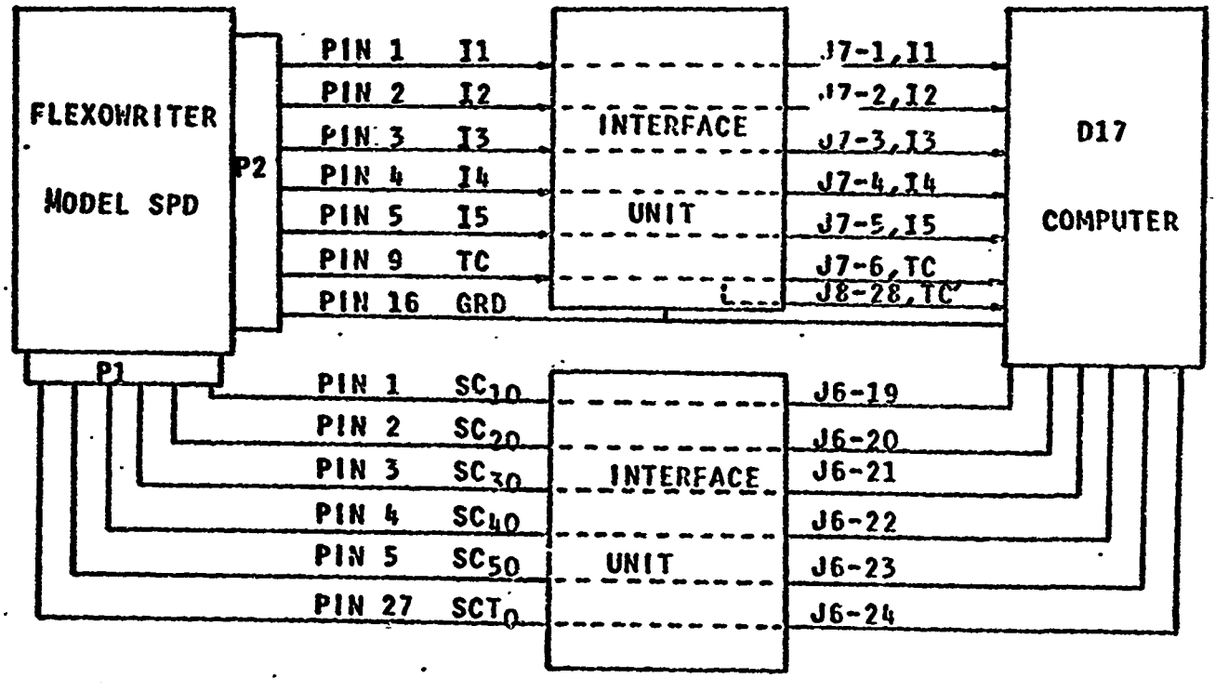
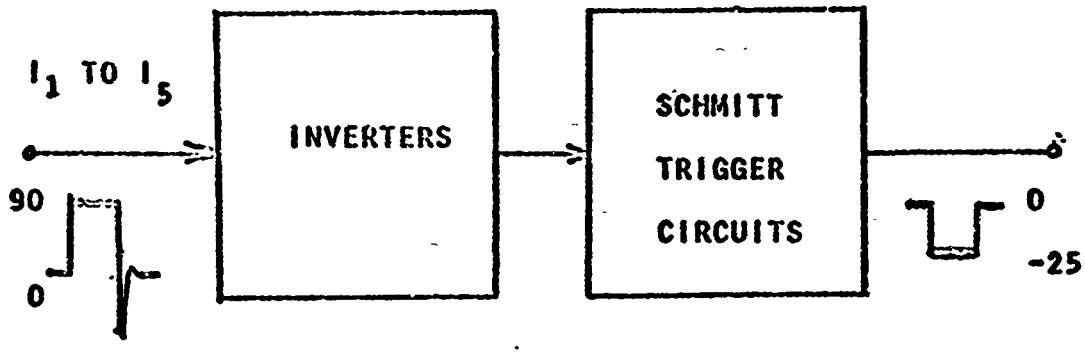


Figure 17. Schematic diagram of the Flexowriter-D17B interface.

INTERFACE

[A] INFORMATION SIGNALS



[B] TIMING PULSE

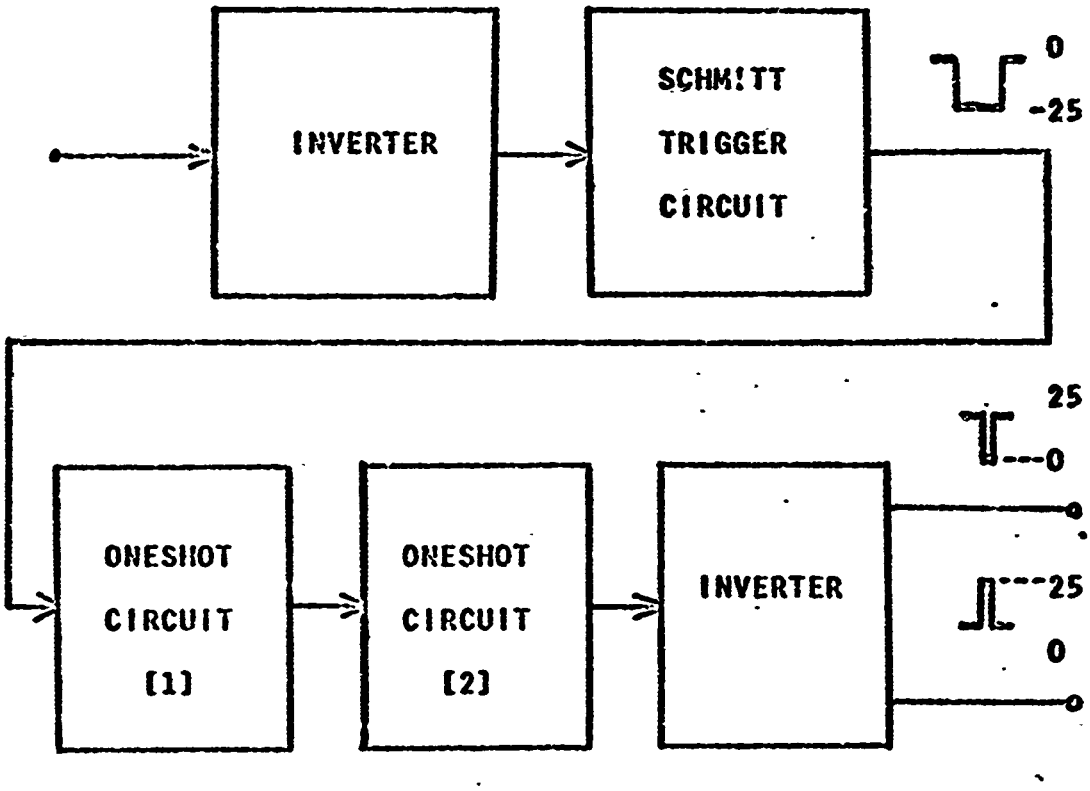


Figure 18. Block diagram of the Flexowriter to D17B interface.

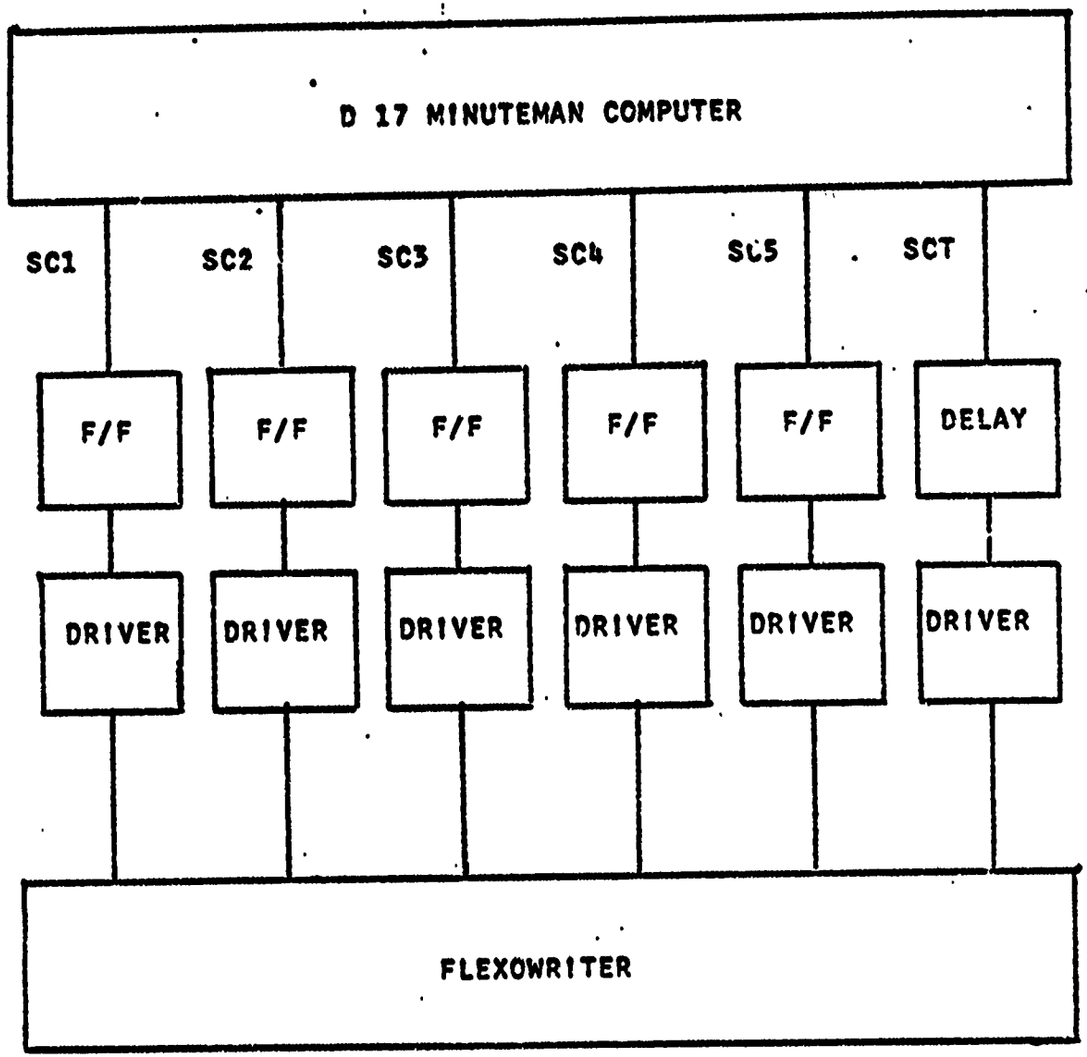


Figure 19. Block diagram of the D17B to Flexowriter interface.

9.0 CONCLUSIONS

Minicomputers are designed primarily for scientific computing such as control, data acquisition, communications, and other dedicated applications, but they have the same basic hardware components as large-scale computers. Although the D17B was designed specifically for use with the Minuteman missile, it exhibits characteristics similar to commercial minicomputers. The cost of developing a D17B system is low enough and it is flexible enough so that it can be used in many new applications areas.

Because of the availability of a large number of D17B computers, the potential exists for spreading the development cost over a large number of computers. There is need for further software development, further peripheral I/O development, and for the development of low-cost peripherals.

Since there is an inherent trade-off between equipment cost and programming effort, it will be desirable to share standard subroutines developed by various users. The I/O capability of the D17B has been found to be particularly suited to real-time applications such as control, data acquisition, and other special-purpose uses. The ease with which any general memory location can be directly addressed is a desirable feature. The lack of speed inherent in a serial computer is partially compensated by the multiprocessing capability.

For general or stand-alone computing applications, the following capabilities are required.

1. Computer must be programmable and capable of modifying the program as a result of calculations.
2. Instruction repertoire must be adequate to perform the desired variety of calculations.
3. Memory must provide for storage of data, program instructions, and the results of calculations.
4. A suitable means must be provided for outputting, recording, and displaying the results of calculations.

The D17B has been programmed to perform the calculations required for navigation, guidance, and control purposes such as numerical integration using Simpson's rule and sine-cosine power series. It has been programmed in the Systems Laboratory for such additional computations as square root, reciprocal, logarithm, and n-th root. Therefore, it is concluded that the D17B meets the requirement of being programmable.

In the missile guidance application, the write heads for the main memory were disabled to provide for memory protect. The necessary logic signals have been determined so that these write heads can be enabled. This permits the flexibility of instruction and address modification under program control.

Many minicomputers offer hardware multiply and divide as options at extra cost. Although the D17B has four hardware multiply instructions, the division operation has been omitted for the purpose of decreasing size and weight. If only a few constants are to be used as divisors, the reciprocals can be precalculated and used in place of the constants. Division by a factor of two can be accomplished by right shifting the data in the accumulator. If the exact value of the data that are to be used as divisors are not known a priori, but the range is known, then a subroutine for the reciprocal can be written. If A is the data word that is to be used as a divisor, then the desired reciprocal A^{-1} can be obtained by an iterative computation involving two multiplications and one subtraction per iteration. Multiplication by the reciprocal can then replace the division operation to complete the complement of arithmetic operations that are normally available. The D17B has both an unconditional transfer instruction and a transfer on minus instruction. This latter instruction can be combined with other instructions to provide other types of transfers. Thus, allowing for the use of certain subroutines, the instruction repertoire is adequate to perform a variety of

calculations. Subroutines must obviously be used for such calculations as square root, logarithm, sine-cosine, and others.

Unless the D17B is modified by increasing the memory capacity or used as a tandem interconnection of several units, then the application to general computing will be limited to those tasks for which 2,727 words of 24-bits or 5,454 words of 11-bits are adequate. I/O interface capability must be provided by the user. The Systems Laboratory has developed a console control panel for manual program input. A flexowriter has been interfaced to provide typewriter keyboard and paper tape input as well as printed output or punched paper tape. A CRT display scope is also available for output monitoring.

In addition to capabilities required for general computing applications, control computing applications require a flexible I/O structure to accomodate a variety of devices. As described in Section 2.3, the I/O capability of the D17B is extremely versatile.

For real-time control applications, the D17B must be able to accept and process input data sufficiently fast that the results of this processing can be used to influence and control the appropriate variables. The D17B was designed to accomplish real-time computation as required for missile guidance; however, the bandwidth of the particular application will dictate the speed requirement. The D17B performed real-time communication with external devices such as the velocity meters, accelerometers, and D-A converters to obtain data and issue commands necessary for navigation, guidance, telemetry, and control functions.

As indicated in the specifications given in Table 1, the D17B has a maximum I/O data rate of 25,600 words per second. Direct data entry is also provided. Hence, within the limits of its capabilities the D17B appears to be very appropriate for a variety of control and special-purpose applications.

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